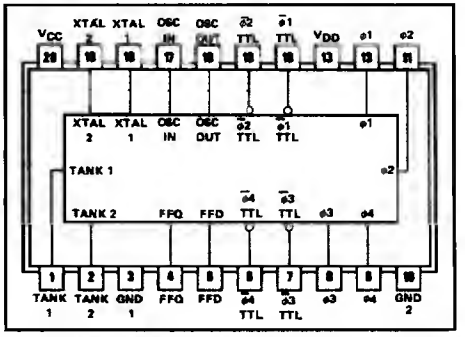
TYPE SN74LS362 (TIM9904)
FOUR-PHASE CLOCK GENERATOR/DRIVER

BULLETIN NO. DL-S 7712476, OCTOBER 1976—REVISED AUGUST 1977

- Clock Generator/Driver for The TMS 9900 or Other Microprocessors
- High-Level 4-Phase Outputs
- Complementary TTL 4-Phase Outputs
- Self-Contained Oscillator Can be Crystal or Capacitor Controlled
- External Oscillator Can Be Used
- Clocked D-Type Flip-Flop With Schmitt-Trigger Input For Reset Signal Synchronization

SN74LS362 . . . J OR N PACKAGE
(TOP VIEW)

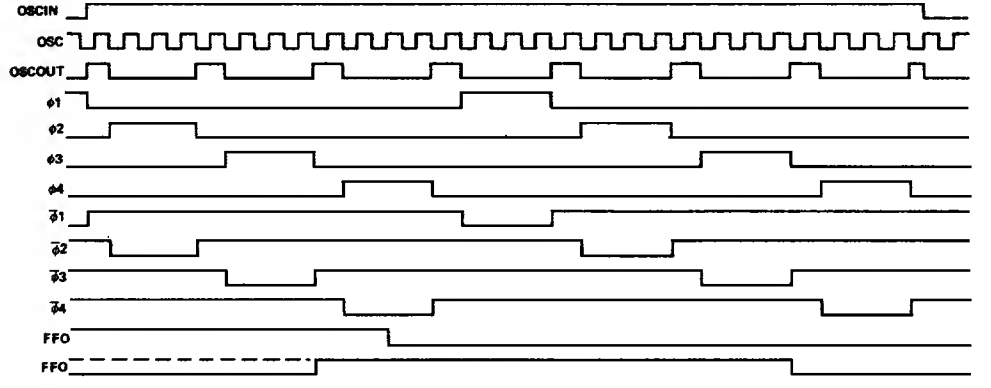


description

The 'LS362 consists of an oscillator, divide-by-four counter, a second divide-by-four counter with gating to generate four clock phases, high-level (12-volt) output drivers, low-level (5-volt) complementary output drivers, and a D-type flip-flop controlled by an external signal and the $\phi 3$ clock. The four high-level clock phases provide clock inputs to a TMS 9900 microprocessor. The four complementary TTL-level clocks can be used to time memory or other logic functions in a TMS 9900 computer system. The D-type flip-flop can be used to provide (for example) a reset signal to a TMS 9900, timed by $\phi 3$, on receipt of an input to the FFD input from power turn-on or a manual switch closure. Other applications are possible. A safety feature has been incorporated in the ϕ outputs such that if an open occurs in the V_{CC} supply common to 'LS362 and TMS 9900, the ϕ outputs will go low thus protecting the TMS 9900.

The frequency of the internal oscillator can be established by a quartz crystal or capacitor and LC circuit. Either a fundamental or overtone crystal may be used. The LC circuit connected to the tank inputs selects the desired crystal overtone or establishes the internal oscillator frequency when a capacitor is used instead of a crystal. An LC circuit must always be used at the tank inputs when using the internal oscillator. An external oscillator can be used, if desired, see "Applications Information" for details.

typical phase relationships of inputs and outputs (OSC is internal)



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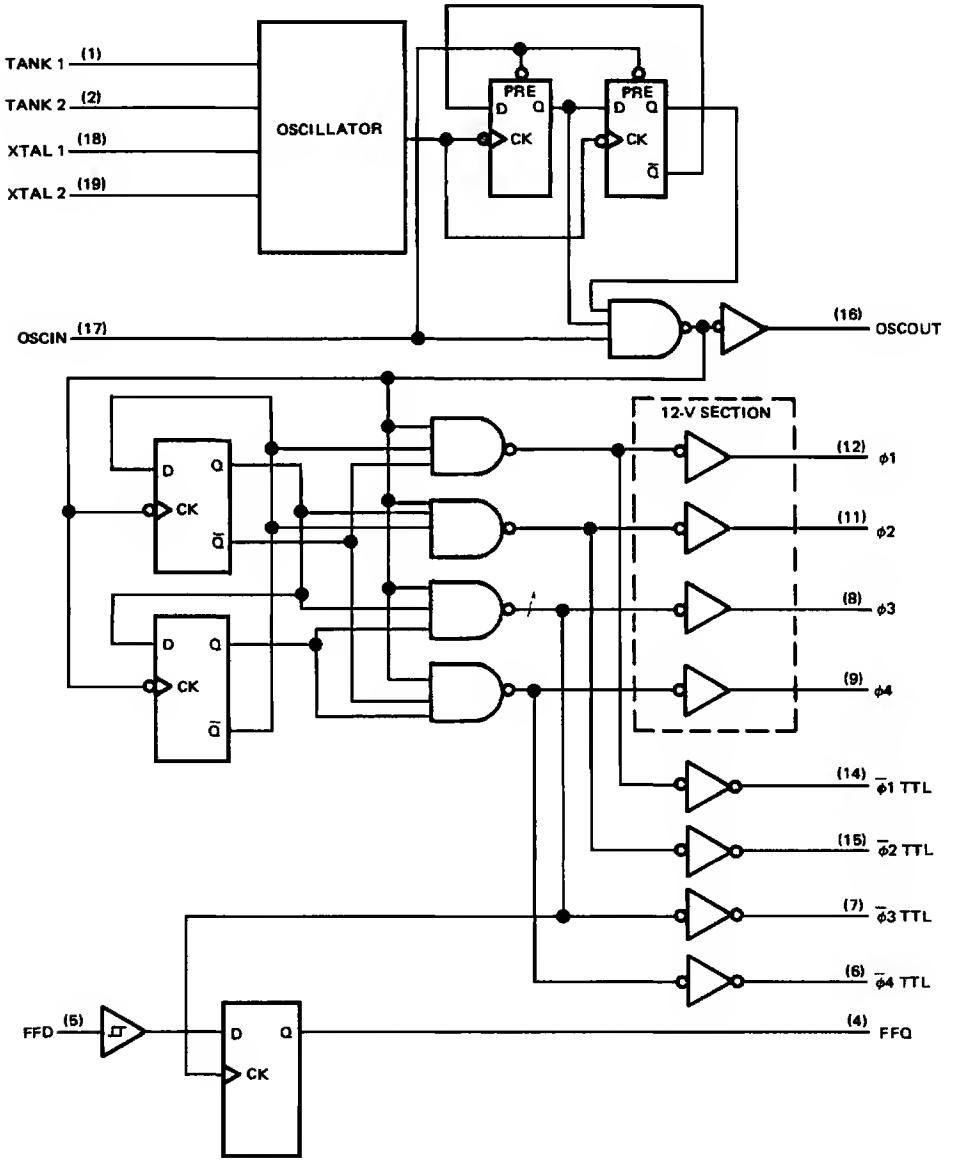
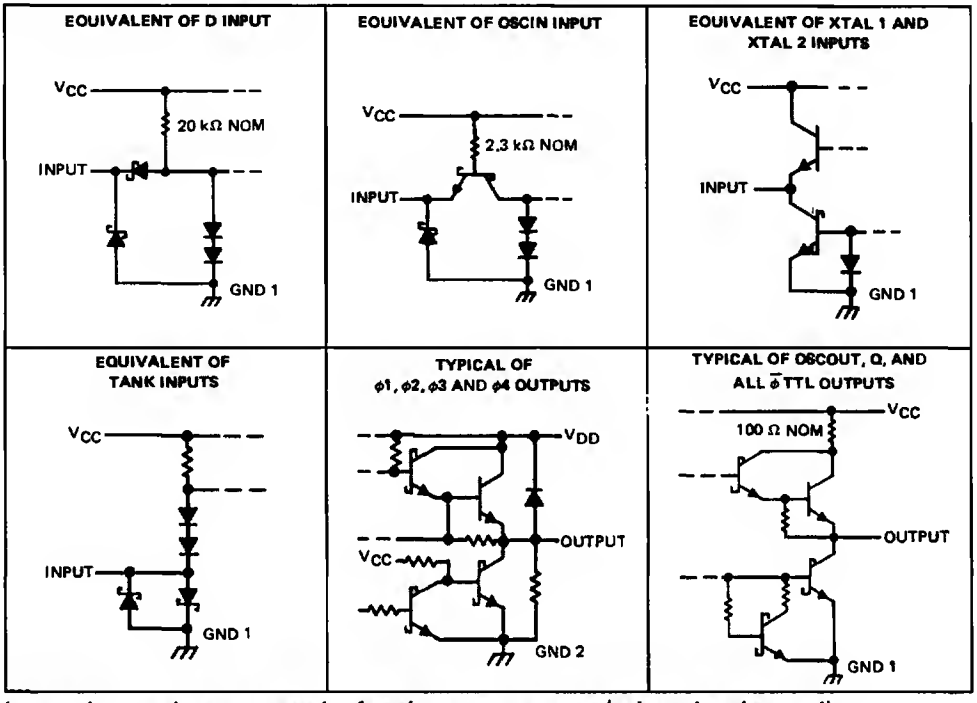
functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC} (see Note 1)	7 V
V_{DD} (see Note 1)	13 V
Input voltage: OSCIN	5.5 V
FFD	−0.5 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminals connected together.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltages	V_{CC}	4.75	5	5.25	V
	V_{DD}	11.4	12	12.6	V
High-level output current, I_{OH}	φ1, φ2, φ3, φ4			−100	μA
	All others			−400	μA
Low-level output current, I_{OL}	φ1, φ2, φ3, φ4			4	mA
	All others			8	mA
Internal oscillator frequency, f_{osc}			48	54	MHz
External oscillator pulse width, $t_{w(osc)}$		25			ns
Setup time, FFD input (with respect to falling edge of φ3), t_{su}		50			ns
Hold time, FFD input (with respect to falling edge of φ3), t_h		−30			ns
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	FFQ					0.5	V
		OSCIN					0.8	
$V_{T+} - V_{T-}$	Hysteresis	FFQ			0.4	0.8		V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, V_{QQ} = 11.4 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	$\phi1, \phi2, \phi3, \phi4$	V_{CC} = 4.75 V,	I_{OH} = −100 μA	V_{QQ}−2	V_{DD}−1.5	V_{DD}	V
		Other outputs	V_{DD} = 11.4 V to 12.6 V	I_{OH} = −400 μA	2.7	3.4		
V_{OL}	Low-level output voltage	$\phi1, \phi2, \phi3, \phi4$	V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_{OL} = 4 mA		0.25	0.4	mA
		Other outputs		I_{OL} = 4 mA		0.25	0.4	
				I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	FFD	V_{CC} = 5.25 V, V_{QQ} = 12.6 V	V_I = 7 V			0.1	mA
		OSCIN		V_I = 5.5 V			0.3	
I_{IH}	High-level input current	FFQ	V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 2.7 V				20	μA
		DSCIN					60	
I_{IL}	Low-level input current	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 0.4 V				−0.4	mA
		DSCIN					−3.2	
I_{OS}	Short-circuit output current‡	All except $\phi1, \phi2, \phi3, \phi4$	V_{CC} = 5.25 V		−20		−100	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.25 V, FFQ and OSCIN at GNQ, Outputs open			105	175	mA
I_{QQ}	Supply current from V_{DQ}		V_{CC} = 5.25 V, V_{QQ} = 12.6 V, FFQ and OSCIN at GNQ, Outputs open			12	20	mA

†All typical values are at V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs $\phi1$, $\phi2$, $\phi3$, and $\phi4$ do not have short-circuit protection.

switching characteristics, T_A = 25°C, V_{CC} = 5 V, V_{DD} = 12 V, f_{osc} = 48 MHz, see figure 1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{out}	Output frequency, any ϕ or $\bar{\phi}$ TTL			3		MHz
f_{out}	Output frequency, OSCOUT			12		MHz
$t_{c(\phi)}$	Cycle time, any ϕ output			333		ns
$t_{r(\phi)}$	Rise time, any ϕ output		5		20	ns
$t_{f(\phi)}$	Fall time, any ϕ output		5		20	ns
$t_{w(\phi)}$	Pulse width, any ϕ output high		40			ns
$t_{\phi1L, \phi2H}$	Delay time, $\phi1$ low to $\phi2$ high		0	5	15	ns
$t_{\phi2L, \phi3H}$	Delay time, $\phi2$ low to $\phi3$ high		0	5	15	ns
$t_{\phi3L, \phi4H}$	Delay time, $\phi3$ low to $\phi4$ high		0	5	15	ns
$t_{\phi4L, \phi1H}$	Delay time, $\phi4$ low to $\phi1$ high	Output loads:	0	5	15	ns
$t_{\phi1H, \phi2H}$	Delay time, $\phi1$ high to $\phi2$ high	$\phi1, \phi3, \phi4$: 100 pF to GND	70	83		ns
$t_{\phi2H, \phi3H}$	Delay time, $\phi2$ high to $\phi3$ high	$\phi2$: 200 pF to GND	70	83		ns
$t_{\phi3H, \phi4H}$	Delay time, $\phi3$ high to $\phi4$ high	Others: R_L = 2 kΩ,	70	83		ns
$t_{\phi4H, \phi1H}$	Delay time, $\phi4$ high to $\phi1$ high	C_L = 15 pF	70	83		ns
$t_{\phi H, \bar{\phi}TL}$	Delay time, ϕ_n high to $\bar{\phi}_n$ TTL low	See Note 2		−8		ns
$t_{\phi L, \bar{\phi}TH}$	Delay time, ϕ_n low to $\bar{\phi}_n$ TTL high			−19		ns
$t_{\phi3L, QH}$	Delay time, $\phi3$ low to FFQ output high			−7		ns
$t_{\phi3L, QL}$	Delay time, $\phi3$ low to FFQ output low			−12		ns
$t_{\phi L, DSOH}$	Delay time, ϕ low to OSCOUT high			−5		ns
$t_{\phi H, DSOL}$	Delay time, FFQ high to QSCDUT low			−13		ns

NOTE 2: Use load circuit for bi-state totem-pole outputs, page 3-11.

PARAMETER MEASUREMENT INFORMATION

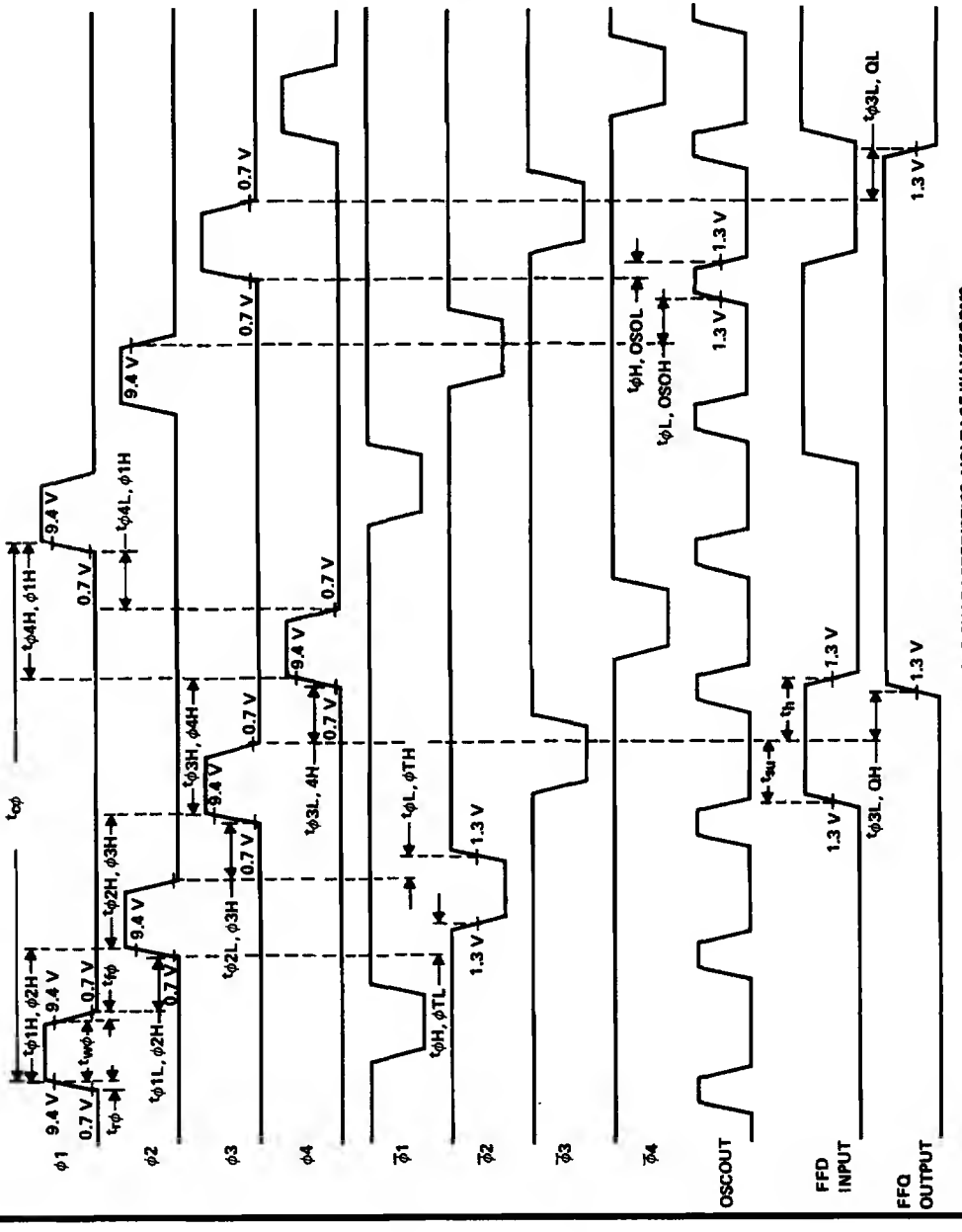

FIGURE 1–SWITCHING CHARACTERISTICS, VOLTAGE WAVEFORMS

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APPLICATION INFORMATION

Figure 2 shows the 'LS362 connected to a TMS9900. The oscillator is shown operating with a quartz crystal and an LC circuit connected to the tank terminals.

For operation of the TMS 9900 microprocessor at 3 MHz, the frequency reference will need a resonant frequency of 48 MHz (16 x 3 MHz). A quartz crystal used as a frequency reference should be made for series-mode operation with a resistance in the 20- to 75-ohm range and be capable of a minimum of 2 *mW* power dissipation. Typical frequency tolerance is ±0.005%. For 48-MHz operation a third-overtone crystal is used. The inductance L connected across the tank terminals should be 0.47 μH ± 10%, and the capacitance C (including board capacity) should be 22 pF ± 5%. The LC circuit should be tuned to the third-overtone crystal frequency for best results. A 0.1-μF capacitor can be substituted for the quartz crystal. With a capacitor rather than a crystal, the LC tuned circuit establishes the operating frequencies. LC component values for operation at any frequency can be computed from $f_{osc} = 1/(2\pi\sqrt{LC})$ where f_{osc} is the oscillator frequency, L is the inductance value in henries, and C is the capacitance value in farads.

When the internal oscillator is being used, OSCIN should be connected to V_{CC} through a resistor (1 kΩ nominal) and an LC tank circuit must be connected to the tank inputs. An external oscillator can be used by connecting it to OSCIN and disabling the internal oscillator by connecting the crystal terminals to V_{CC} and leaving the tank inputs open. An external oscillator must have a frequency four times the desired output clock frequency and a 25% duty cycle. See Figure 3.

The first low-level external clock pulse will preset the divide-by-four counter, allowing the external oscillator signal to directly drive the phase generator. Figure 3 is a timing diagram illustrating operation with an external oscillator.

Resistors between $\phi1$, $\phi2$, $\phi3$, and $\phi4$ outputs of the 'LS362 and the corresponding clock input terminals of the TMS 9900 should be in the 10- to 20-ohm range (See Figure 2). Their purpose is to minimize overshoot and undershoot. The required resistance value is dependent on circuit layout. Clock signal interconnections should be as short as possible.

The D-type flip-flop associated with pins FFD and FFQ can be used to provide a power-on reset and a manual reset to the TMS 9900 as shown in Figure 4. A Schmitt-trigger circuit driving the D input generates a fast-rising waveform when the input voltage rises to a specific value. At power turn-on, voltage across the 0.1 μF capacitor in Figure 4 will rise towards V_{CC}. This circuit provides a delay that resets the TMS 9900 after V_{CC} has stabilized. An optional manual reset switch can be connected to the delay circuit for resetting the TMS 9900 at any time. The TMS 9900 HOLD signal could alternately be actuated by FFD.

The ground terminals GND1 and GND2 should be connected together and to system ground.

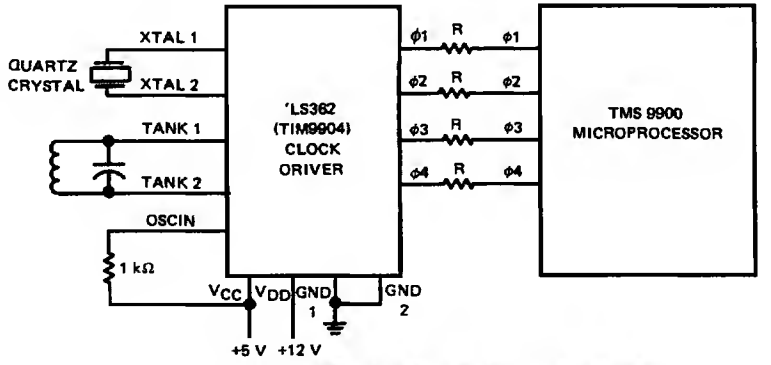

FIGURE 2—'LS362 CRYSTAL-CONTROLLED OPERATION

APPLICATION INFORMATION

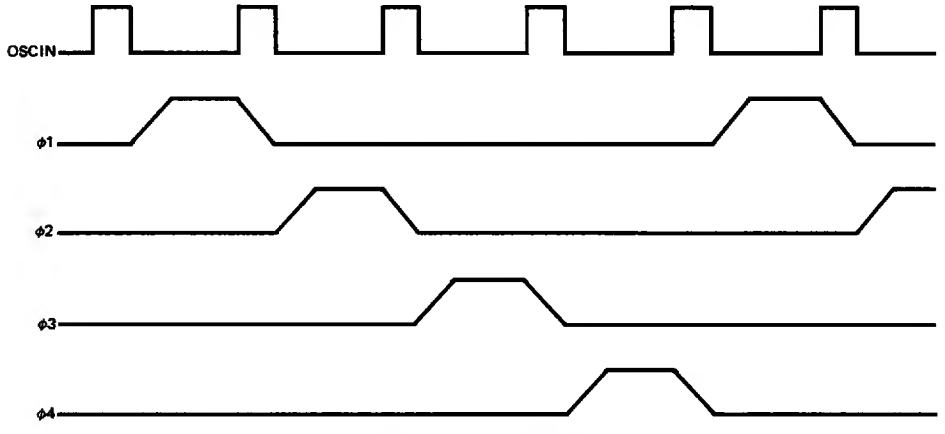

FIGURE 3–EXTERNAL OSCILLATOR TIMING

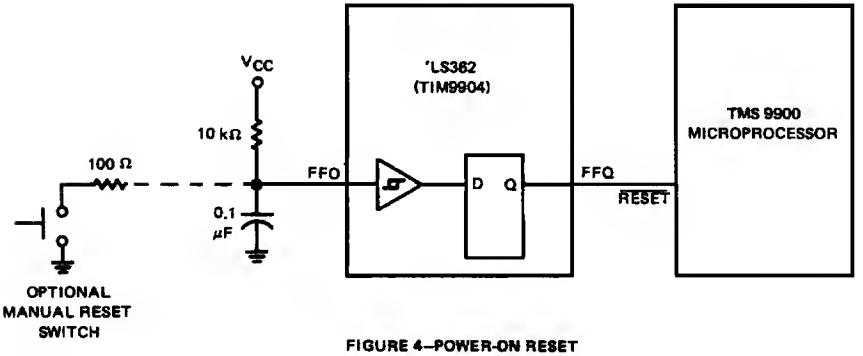

FIGURE 4–POWER-ON RESET

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